4.5 A 0.13µm 1.5V CMOS I/Q Downconverter with Digital Adaptive IIP2 Calibration

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Second-order intermodulation distortion (IMD2) is a significant impairment in direct-conversion and low-IF receivers. In order to fulfill tough IIP2 requirements present in many wireless systems, some type of on-chip even-order distortion cancellation is necessary, either in the form of compensation of distortion or calibration of mismatches responsible for statistical nature of IIP2. The latter technique is preferable, as it exploits existing receiver nonlinearities. The basic idea behind IP2 calibration is to introduce intentional mismatch in the RX mixer, being the main contributor to IMD2, in order to cancel the impact of existing mismatches by converting part of the common-mode distortion to differential mode [1]. Since mixer mismatches are sensitive to operating conditions including temperature, voltage supply, LO frequency, and even RF blocker frequency [2], IP2 calibration settings have to be updated, either periodically or continuously, in order to maintain high linearity. This paper describes an implementation of the IP2 calibration scheme introduced in [3] and a modified version of it that facilitate continuous background mixer recalibration.

The proposed IP2 improvement system architecture is depicted in Fig. 4.5.1. It can be regarded as a mixed-signal embodiment of the adaptive interference cancellation architecture. A mixer equipped with an IP2 tuner downconverts the RF input signal to a differential IF output signal. As a by-product of active device second-order nonlinearities, the common-mode output signal contains second-order distortion, which can be detected and correlated with the differential output signal in order to estimate the differential second-order distortion. The correlation is carried out by an adaptive LMS block in the digital domain. This is critical to the successful calibration as digital circuits are inherently free of mismatches. The LMS block updates the codes of the IP2 tuner in order to minimize the output differential distortion. Compared with compensation architectures, the proposed system does not require any envelope squaring block.

Intentional mismatches can be introduced in various parts of the mixer [3]. Due to noise considerations, the IP2 tuner used in this work is placed in the output stage of the mixer. Shown in Fig. 4.5.2, the tuner is combined with the output common-mode feedback block (CMFB). It converts digital tuning codes into analog mismatch between widths of the current sources. IMD2 cancellation is performed entirely in the current domain, taking advantage of the fact that the implemented mixer is based on a current-mode output architecture providing high linearity at low voltage supply. A feature of the presented IP2 tuner topology is the merged IP2 and DC tuning architecture, which reduces static DC offsets generated by the IP2 tuner while maintaining good balance by equally loading the output branches of the mixer switching stage. By simultaneously changing the IP2 and DC tuner settings, baseband transient signals due to input step signals are significantly reduced, which is desirable for online calibration. The reference signal for adaptive calibration is derived from the output signal of the CMFB block, using a detection circuit presented in Fig. 4.5.3.

The diagram of the digital section is depicted in Fig. 4.5.4. It consists of sign comparators for low-pass filtered mixer differential and common-mode output signals as well as a low-complexity sign-sign LMS adaptation block, which results in a simple hardware implementation, at the expense of decreased convergence speed and poorer IMD2 suppression in the steady state. 8b inner and outer up/down counters are used. When the inner counter under- or overflows, the outer counter is updated while the inner counter is reset to half of its maximum value. This technique smooths the algorithm convergence and makes it more robust against baseband transients. Comparators contain additional adaptive loops (not shown in Fig. 4.5.4) for canceling static DC offsets that would otherwise impair their distortion detection capabilities.

The I/Q downconverter with digital adaptive equalizer is fabricated in a 0.13µm RF CMOS process. The chip contains I/Q Gilbert cell mixers with current-mode interface to baseband built around fully differential opamps forming a 1-pole filter, a divide-by-2 circuit for generating quadrature LO signals from a signal at twice the LO frequency, IP2 tuners, opamp-RC biquad baseband filters with static DC-offset compensation and 20dB of gain, signal comparators as well as digital logic and biasing circuitry. The chip draws 48mA from a 1.5V supply at 2GHz LO frequency. The total small-signal gain is 53dB in the middle of the 1.5MHz-wide passband. The downconverter has an out-of-band 1dB compression point of 3dBm and IIP3 of 12dBm. Double-sideband input-referred noise voltage spectral density is 5.1nV/√Hz at 100kHz offset and 3.2nV/√Hz at 1MHz offset.

Figure 4.5.5 presents measured IIP2 improvement curves for one test chip but operating at different conditions. The reference curve corresponds to a 2GHz LO frequency and two-tone RF blocker situated 150MHz above the LO frequency. Other curves are obtained for different LO frequency (1GHz), different RF blocker frequency (150MHz below the LO frequency) and different voltage supply (1.4V). It can be seen that optimum tuning codes differ, confirming the necessity of recalibration in order to maintain high linearity. To check the transient behavior of the implemented adaptive calibration system, strong AM modulated out-of-band blocker is fed to the mixer input along with a weak in-band sinusoid. Figure 4.5.6 presents oscilloscope plots of both I and Q output baseband signals. The plots show the reduction of distortion in time, leaving the desired in-band signal intact. Figure 4.5.7 shows the chip micrograph. The die area is 2mm^2, including bond pads.

Acknowledgements:
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References:
[1] K. Kivekäs, A. Pärssinen, and K.A.I. Halonen, "Characterization of IIP2 and DC-Offsets in Transconductance Mixers," *IEEE Trans. Circuits and Systems II*, vol. 48, pp. 1028-1038, Nov., 2001.
[2] D. Manstretta, M. Brandolini, and F. Svelto, "Second-Order Intermodulation Mechanisms in CMOS Downconverters," *IEEE J. Solid-State Circuits*, vol. 38, pp. 394-406, March, 2003.
[3] K. Dufrene and R. Weigel, "Adaptive IP2 Calibration Scheme for Direct-Conversion Receivers," *Proc. IEEE Radio and Wireless Symp.*, pp. 111-114, Jan., 2006.

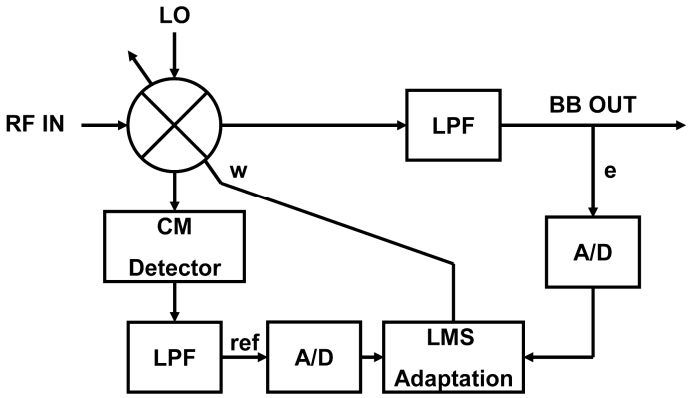

Figure 4.5.1: System architecture.

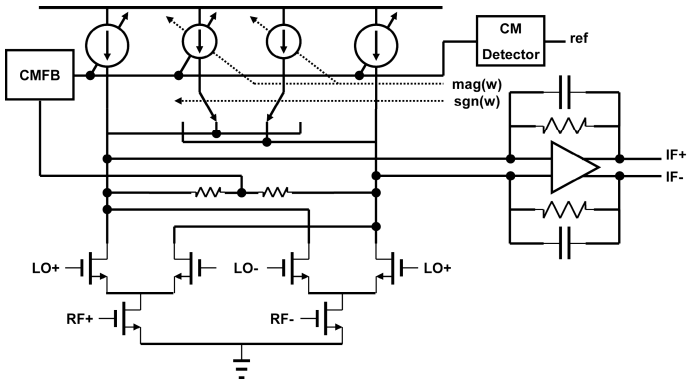

Figure 4.5.2: Mixer with merged IP2 and DC-offset tuner.

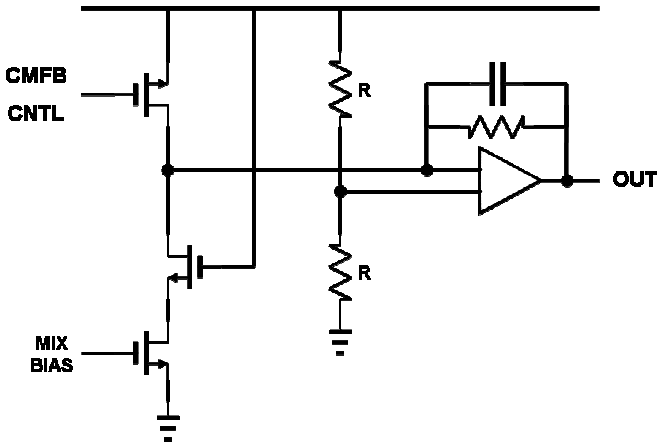

Figure 4.5.3: Common-mode detector.

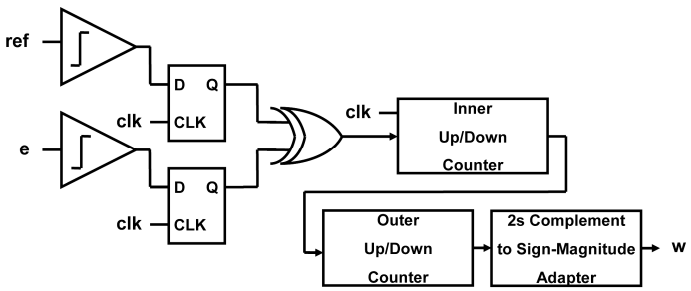

Figure 4.5.4: SS-LMS adaptation circuit.

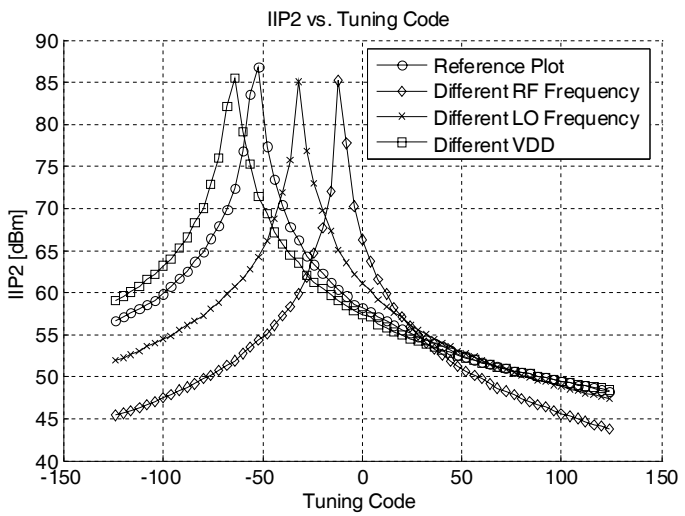

Figure 4.5.5: IP2 improvement curves.

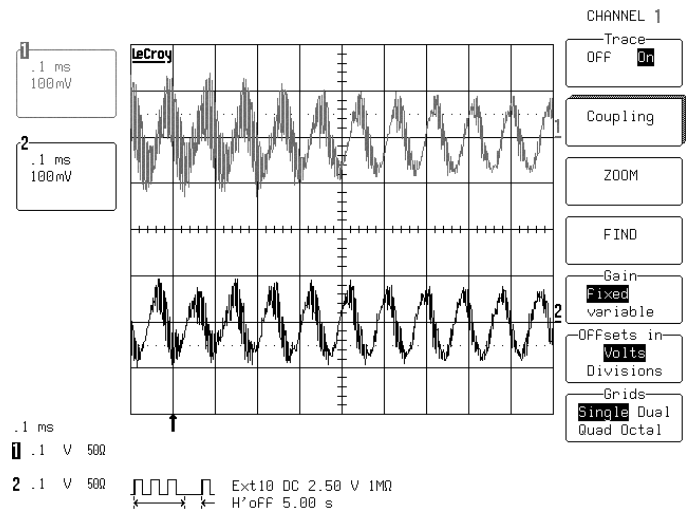

Figure 4.5.6: Transient behavior.

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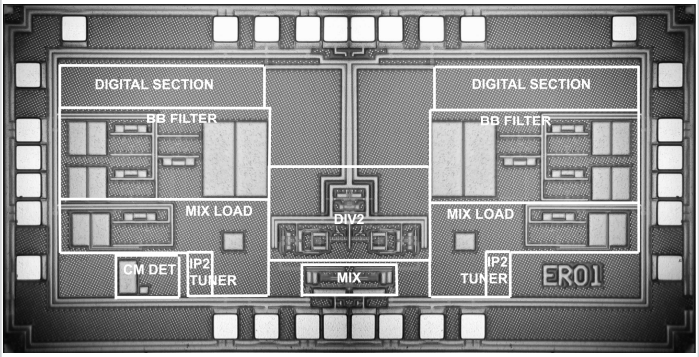

Figure 4.5.7: Chip micrograph.

